A LOW NOISE HETERODYNE 89 GHZ MMIC MODULE FOR THE MULTIFREQUENCY IMAGING MICROWAVE RADIOMETER (MIMR)

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Abstract

The contribution describes the topology of the heterodyne 89 GHz channel of the Multifrequency Imaging Microwave Radiometer (MIMR). Several components such as double sideband 89 GHz mixer, 44.5 GHz local oscillator, frequency doubler, and IF low noise amplifier are realized using monolithic millimeter- and microwave technology. Detector and band-defining low-pass filter are lumped element assemblies. The frontend concept yields a compact low power consuming module with a proposed overall noise figure of about 5.5 dB. A gain of 52 dB is expected between the 89.1 GHz ± 2.7 GHz RF input and the 0.1 GHz - 2.7 GHz IF output.

Introduction

The multifrequency radiometer MIMR to be embarked on the METOP Polar Platform mission in the frame of the POEM (Polar Orbit Earth Mission) program of the European Space Agency (ESA) includes six radiometer receiver subsystems. For the highest frequency subsystem located at 89 GHz a demonstrator is realized using MMIC technology in order to mimimize DC power consumption, mass, and volume. In Fig. 1 the block diagram of the MIMR 89 GHz fronted is shown. In contrast to the most other MMIC radiometer modules published earlier |1, 2| a superheterodyne architecture is chosen. The frequency range is 89 GHz ± 2.7 GHz using a double sideband mixer topology. The local oscillator is operated at 44.5 GHz via a frequency doubler. To fulfil the high requirements concerning noise figure, gain linearity and flatness, appropriate MMIC technologies have to be used for the specific monolithic subcomponents. The following devices are realized using the 0.25 µm MESFET compatible buried layer technology (BE025 technology) of the Daimler-Benz foundry:

- a low noise 89 GHz DSB mixer (DSB noise figure to be less than 4 dB)
- a 44.5 GHz frequency doubler (conversion loss smaller 10 dB)
- an IF monitor coupler 13 dB between 0.1 GHz and 3 GHz

Quarter micron pseudomorphic HFET technology (H2025 technology) is used for

- the low noise IF amplifier 0.1 GHz - 3 GHz (gain >30 dB, noise figure 1.5 dB)
- the variable gain amplifier 0.1 GHz - 3 GHz (gain >25 dB)
- the buffer amplifier 44.5 GHz (1 dB compression point >17 dBm)
- the dielectrically stabilized oscillator DRO (output power >5 dBm).

The band-defining low-pass filter and the detector circuitry are lumped element assemblies. In the following design and measurement results of the single sub-components are shown and expected overall frontend performances are presented.

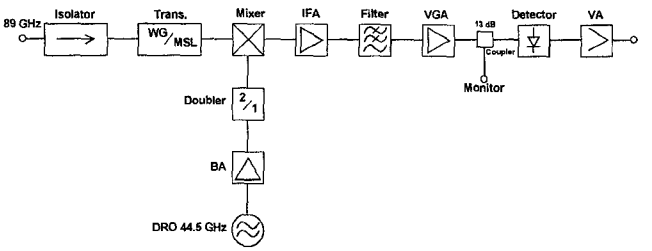

Fig. 1: Block diagram of the MIMR 89 GHz frontend

DSB mixer

For the mixer simulation a non-linear diode model based on the physical understanding of the fabricated Schottky diode is used |3|. A single balanced configuration is chosen because of superior AM noise and LO to RF signal isolation performances. The mixer operates in self bias mode. Matching networks are foreseen for reduction of the needed LO power and for LO and RF matching considerations. At the IF output a band reject filter realized with a radial stub reduces the amount of LO signal. The employed 180° rat race coupler yields excellent isolation between LO and RF ports and allows a very compact design. A photo of the realized chip is shown in Fig. 2. The chip size is 1.5 mm x 1 mm, the substrate height 100 µm. The measured RF performances of the device are plotted in Fig. 3. Optimum conversion loss of about 6.1 dB and DSB noise figure of 3.1 dB are measured at an LO power of 8 dBm. The LO to RF isolation here is better than 21 dB as to be seen in Fig. 4.

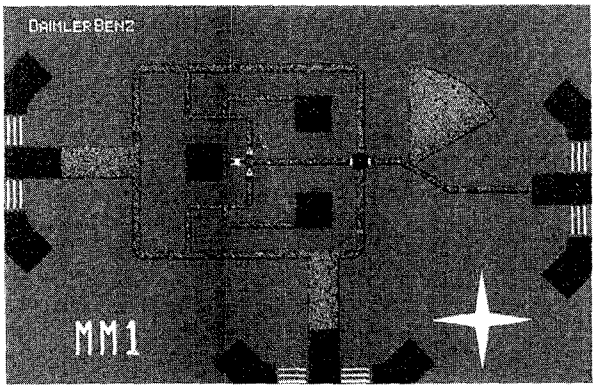

Fig.2: DSB mixer chip

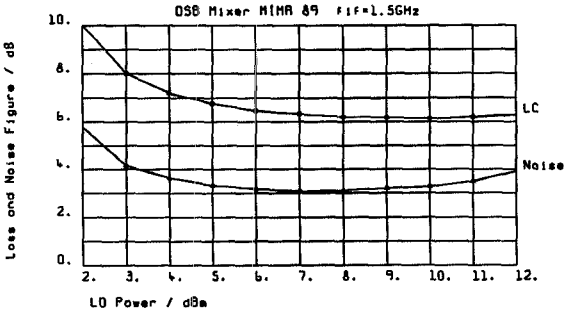

Fig.3: Conversion loss and noise figure of the DSB mixer

Doubler

A schematic of the doubler is given in Fig. 5. It operates in self bias mode. A resistance is introduced in series to the diode for defining the optimum DC operating point. The doubling function is obtained from the nonlinear diode intrinsic conductance and capacitance. The microstrips L5 and L4 are providing short circuits at the diode ports for the frequencies 44.5 GHz and 89 GHz, respectively. Input and output matching networks are realized with single stubs. Fig. 6 shows the Schottky diode doubler chip corresponding to the principle schematic presented in Fig. 5. The chip size is 1.35 mm x 1.1 mm on a 100µm thick GaAs substrate. A large diode with 6 fingers is used in the design in order to handle input power up to 20 dBm. The conversion loss measured at an input frequency of

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44.5 GHz is plotted in Fig. 7 as a function of input power. A loss of 6.7 dB is achieved at power levels higher 12 dBm.

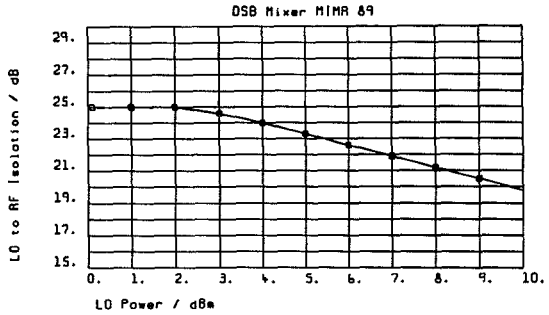

Fig.4: Mixer LO to RF isolation

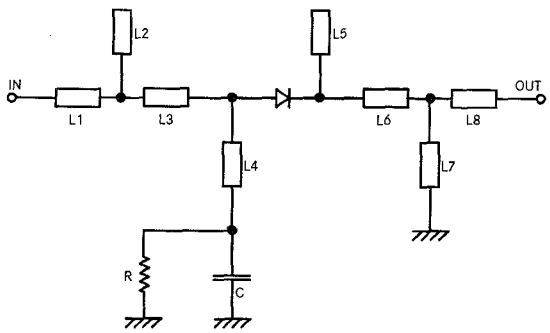

Fig. 5: Principle schematic of the Schottky diode doubler

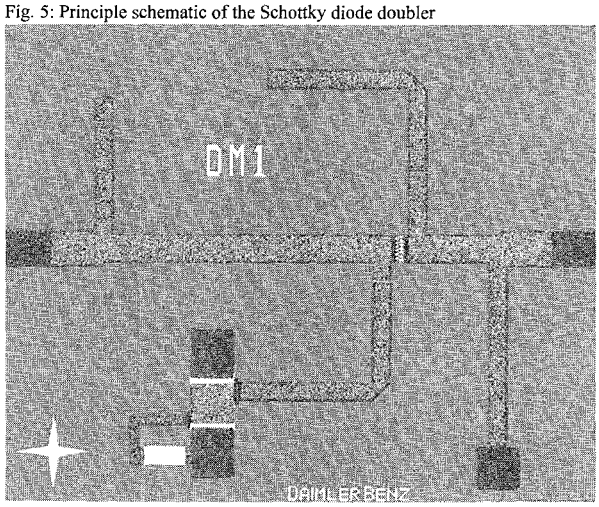

Fig. 6: Doubler chip 44.5 GHz

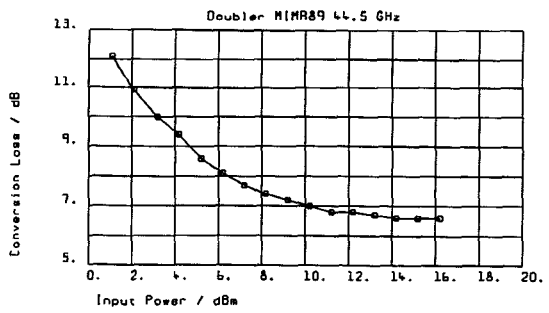

Fig. 7: Conversion loss of the 44.5 GHz doubler

IF Monitor coupler

The coupler consists of a resistive power divider and 6 dB attenuator. The chosen resistors are thin film devices with a sheet resistance of 30 Ω per square. Return loss of the 3 ports is below 20 dB. Transmission loss is 6 dB and coupling loss around 12.5 dB. Fig. 8 shows the layout of the coupler, a combination of power divider and attenuator. The chip size is 1.1 mm x 0.85 mm.

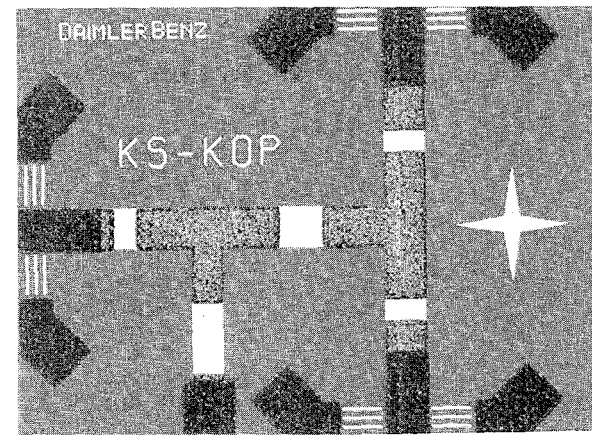

Fig. 8: IF coupler chip

IF LNA

The IF LNA performs a very low noise amplification on a ultrawide IF frequency bandwidth, ranging from 100 MHz to 3 GHz. As active devices high electron mobility transistors with a gate length of 0.25µm and gate width of 480µm (8x60µm) for the first amplifier stage and 120µm (6x20µm) for the second and third amplifier stage are chosen. The transistor in the first amplifier stage has an inductive series feedback from source to ground (for noise matching) and a parallel RC-feedback from drain to gate (for stabilization). The second and third amplifier stages have only parallel feedback. For the realization of the matching networks, combinations of inductances in series and capacitances in parallel are used. A total gain of 35 dB with a gain flatness of ± 0.5 dB is measured from 100 MHz to 2.7 GHz. The output return loss is better or equal 10 dB and the input return loss is better than 8 dB from 100 MHz to 2.7 GHz. The measured noise figure is in the range of 1.5 dB (Fig. 9). A photograph of the chip (3.1 mm x 2.5 mm) is shown in Fig. 10.

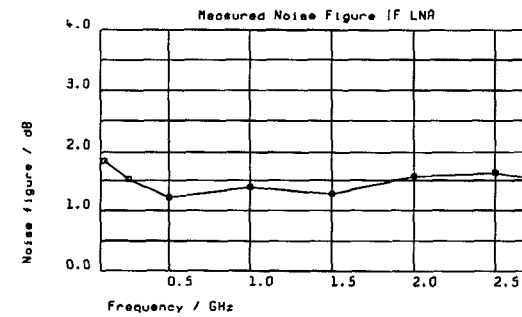

Fig. 9: Measured IF LNA noise figure

IF VGA

A second IF-amplifier is designed as variable gain amplifier VGA. The VGA has very similar specs except that a higher noise figure is tolerable. The design is based on the IF LNA design, whereby the single-gate PMHFET in the second transistor stage is replaced by a dual-gate PMHFET (same gate width of 6x20µm). The gain of the VGA can be controlled by the voltage applied to gate2. A gain of 33.7 dB and 26.0 dB with a gain flatness of ± 0.5 dB is obtained at dual-gate bias conditions of 0 V and -0.6 V, respectively (see Fig. 11). The VGA chip (3.1 mm x 2.5 mm) is presented in Fig. 12.

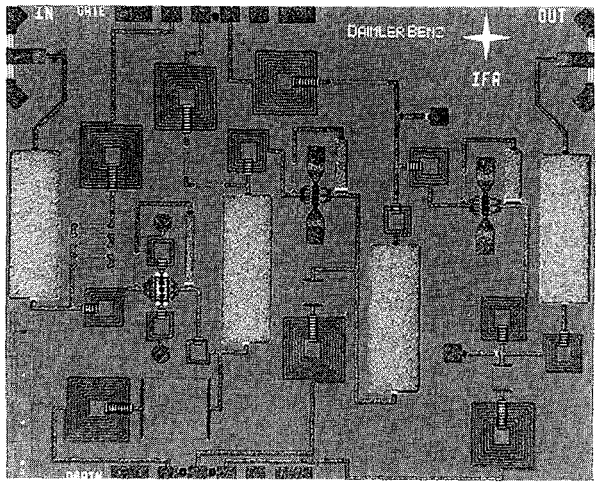

Fig.10: Photograph of the IF LNA chip

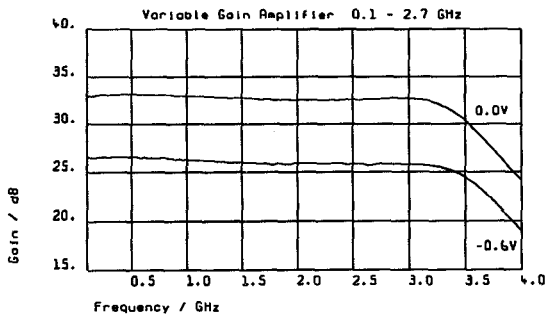

Fig. 11: Gain of the VGA at controll voltages of 0 V and -0.6V

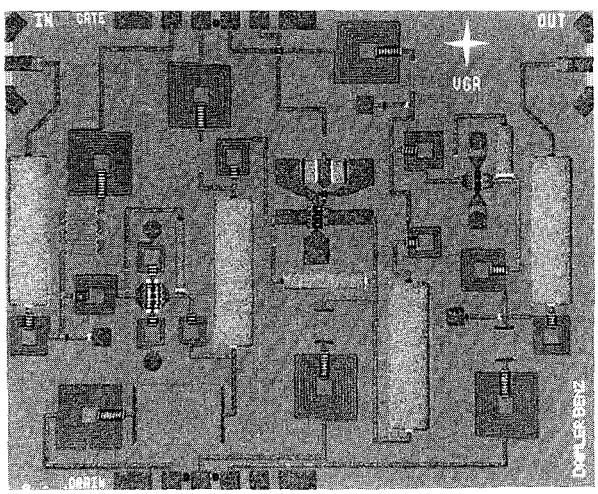

Fig. 12: Photograph of the VGA chip

Buffer amplifier

The basis of the buffer amplifier design is a FET model derived from temperature dependent S-parameter measurements of PMHFETs in microstrip design up to 50 GHz. The buffer amplifier is designed as dual three stage amplifier in parallel. The first and second stage of each amplifier branch contains a PMHFET with 120µm gate width (6 finger with 20µm width). To achieve an output power of 21 dBm a PMHFET with a gate width of 240µm (8 finger with 30µm width) is applied in the output stage of each amplifier branch. To avoid oscillations at lower frequencies, each amplifier stage is designed with respect to unconditional stability. To obtain this, resistive losses are added for lower frequencies. The gate and drain bias networks are RF grounded quarter wavelength stubs at 44.5 GHz. The interstage and output matching is realized by transmission lines. For the input match an open stub in combination with a transmission line is applied to achieve a reasonable frequency bandwidth. Fig. 13 shows the photograph of the dual three stage buffer amplifier with a chip size of 2.5 mm x 2.5 mm. The following amplifier properties are determined at 44.5 GHz:

Small signal gain	13 dB
Input return loss	> 10 dB
Saturation power	> 18 dBm

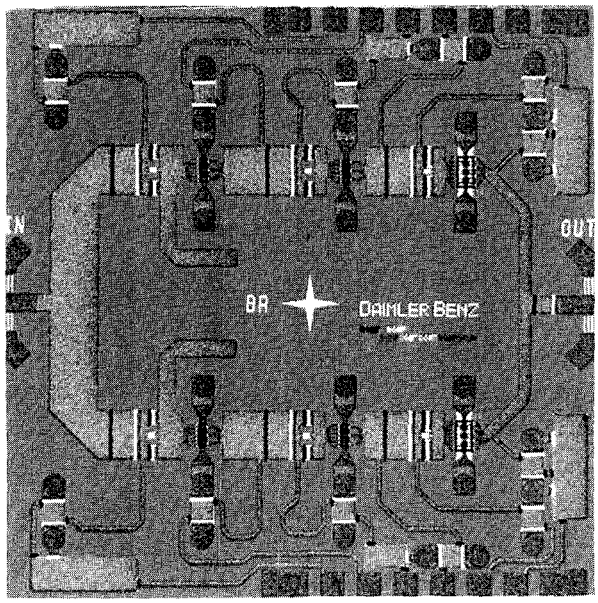

Fig. 13: Buffer amplifier chip

DRO

For the design of the monolithic 44.5 GHz DRO an oscillator topology with a series feedback configuration and the PMHFET in common source operation is chosen, which has been applied with excellent results up to 60 GHz |4|. The dielectrical resonator is placed at the gate side of the transistor, whereas the output port is at the drain side. The length between resonator coupling locus and gate are optimised to obtain maximum negative resistance at the PMHFET drain. The microstrip circuit (chip size 2.5 mm x 1.0 mm) is designed using small signal S-parameters of the PMHEMT (in a special feedback configuration) measured up to 50 GHz and inhouse developed linear CAD software. The dielectric resonator coupled to the microstrip line is modelled as a parallel resonant circuit. Using a resonator with a constant of 35, the diameter of the puck is 1.3 mm and the height 0.6 mm. In Fig. 14 the DRO chip is shown. For measurements the resonator is placed on a carrier substrate adhered close to the active circuit. At 44.5 GHz an output power of + 5 dBm is measured. The spectrum of the oscillator is presented in Fig 15 (phase noise at 100 kHz offset is about -85 dBc/Hz).

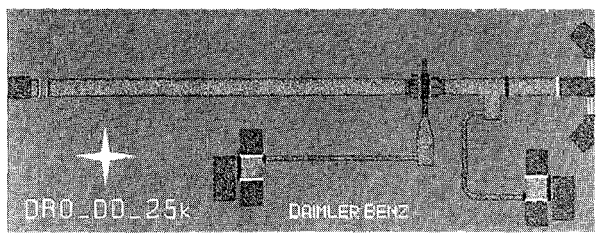

Fig. 14: DRO chip

IF filter

The IF low-pass filter is a 9 pole design requiring the implementation of quasi-lumped series inductances and shunt capacitances. Whereas the capacitances are realized using commercially available MIS chips placed on carrier, for the series inductances quasi - TEM transmission lines with high characteristic impedance are needed. To fulfil this requirement, shielded triplate line sections with air dielectric are introduced. A miniaturized version uses lumped inductors (miniature air coils) instead. The center conductor is a 25µm circular shaped bond wire. The high impedance sections are formed by 1 mm deep milled recesses in a filter housing

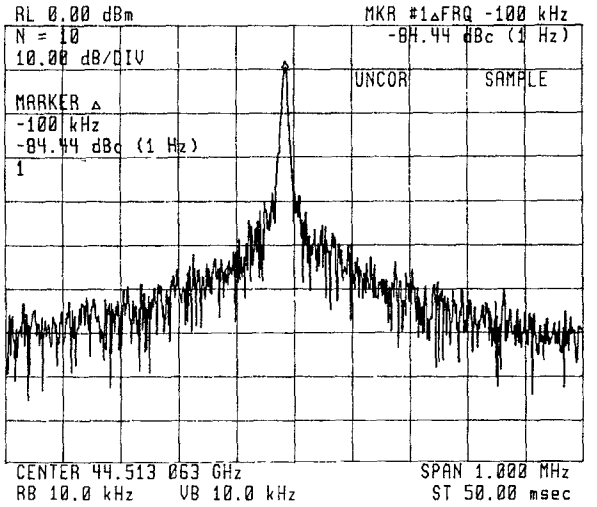

Fig 15: DRO output spectrum

carrier and cover plate. In Fig 16 the measured response of the filter is shown First spurious responses are measured at 27 GHz The realized device is a 32 mm x 10 mm x 6 mm fully shielded Covar block

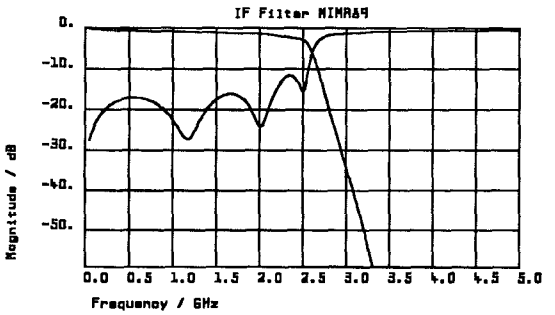

Fig 16: Measured response of the IF filter

Detector circuitry

The detector circuit schematic is shown in Fig. 17. In order to achieve high linearity and low flicker noise behavior SIMMWIC Schottky diodes realized at the Daimler-Benz Research Center are used The video signal is extracted via the series resistor R_S and the shunt capacitor C_2. The detector diode D_1 is forward biased A second diode D_2 is employed for temperature compensation. Nonlinear PSPICE simulations of the equivalent circuit in Fig 17 are carried out to optimize the values of C_1, C_2, and R_S with respect to linearity and flat frequency response For this purpose the diode I/V characteristics are measured at three different temperatures and a nonlinear PSPICE diode model is established. The diodes D_1 and D_2 are connected to a differential video amplifier board via the resistors R_S. The video amplifier contains commercially available OP470 devices (PMI) and is designed to minimize temperature drift effects

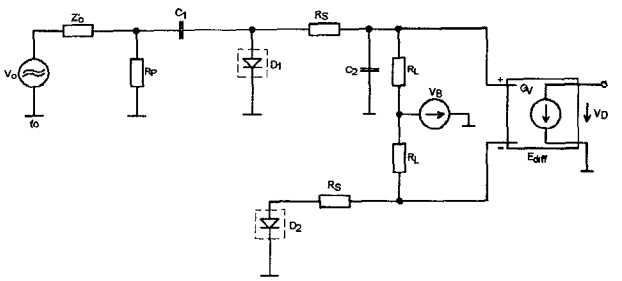

Fig 17· Detector circuit schematic

Frontend overall performances

Taking the above presented measurement results of the single sub-components into account and cascading the RF chain as shown in Fig 1 from the waveguide-to-microstrip transition [5] (transmission loss 0.6 dB) up to the coupler an overall gain and noise figure of the frontend can be predicted. Fig. 18 shows the results for a VGA control voltage of -0 6V to be adjusted due to the optimum linearity condition of the detector. The gain between 0.1 GHz and 2.7 GHz shows a value of about 52 dB with a ripple of ± 0.6 dB, the associated noise figure is between 5.3 dB and 5 7 dB These figures are valid for a baseplate temperature of 25°C.

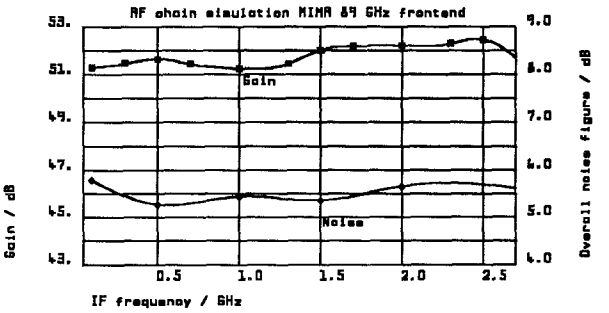

Fig 18: Simulation of the radiometer RF chain

Conclusion

In this paper a set of components for a 89 GHz radiometer fronted is presented Most of the components are monolithic microwave and millimeter wave GaAs integrated circuits using MESFET compatible buried layer technology as well as quarter-micron PMHFET technology A simulated overall noise figure for the frontend in the range of 5.5 dB is based on measurement results of the presented components. The expected overall gain is higher than 52 dB

Acknowledgement

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